

## Programmable V.11/V.35 Transceiver

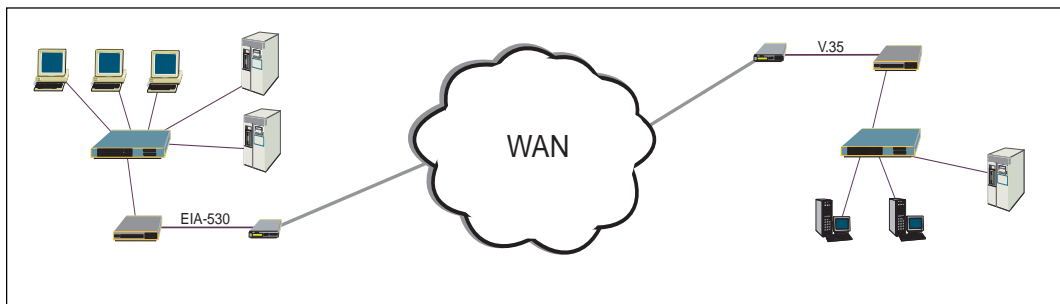
- +5V Only Operation
- Programmable V.11 or V.35 Selection
- Three Differential V.11 Transceivers in V.11 Mode
- Three Differential V.35 Transceivers in V.35 Mode
- No External Resistor Termination for Compliant V.35 Operation
- V.11 Cable Termination (approx. 120Ω) Internally Configured in V.11 Mode
- Tri-State capability on drivers and receivers
- Ideal low cost solution for X.25 or Frame Relay Serial Ports



### DESCRIPTION

The **SP322** is a programmable V.11 or V.35 transceiver IC. The **SP322** contains three drivers and three receivers when selected in each mode. The selection is done by the  $\overline{V.11/V.35}$  select pin. The V.11 transceivers can typically operate at 10Mbps while adhering to the ITU V.11 specifications. The V.35 transceivers can operate up to 10Mbps while adhering to the ITU V.35 specifications.

The **SP322** contains internal resistor termination for compliant V.35 operation as well as the V.11 termination on the receiver inputs for optional cable termination. Each **SP322** driver contains a control pin which disables the output and places the output pins in a high impedance state. Each receiver also has a control pin which places the receiver outputs in a high impedance state. The enable pins will disconnect the internal termination network for whichever mode the **SP322** is selected. For the receivers, the enable pin will place the input pins in a high impedance (approx. 15kΩ). This allows for convenient DTE-DCE configuration by connecting the driver outputs to the receiver inputs, thus allowing the enable pins to select the desired DTE or DCE operation.



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

$V_{CC}$ .....+7V  
 Storage Temperature.....-65°C to +150°C  
 Power Dissipation  
     44-pin Plastic QFP.....1500mW  
 Package Derating:  
 44-pin Plastic QFP  
      $\theta_{JA}$ .....52°C/W



**CAUTION:**  
 ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

## SPECIFICATIONS

Typically 25°C @  $V_{CC}$  = +5V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>LOGIC INPUTS</b>					
$V_{IL}$ $V_{IH}$	2.0		0.8	Volts Volts	
<b>LOGIC OUTPUTS</b>					
$V_{OL}$ $V_{OH}$	2.4		0.4	Volts Volts	$I_{OUT} = -3.2mA$ $I_{OUT} = 1.0mA$
<b>V.35 DRIVER</b>					
<b><u>DC Characteristics</u></b>					
Outputs					
Test Terminated Voltage	±0.44	±0.55	±0.66	Volts	per Figure 10
Source Impedance	50	100	150	$\Omega$	per Figure 11
Short Circuit Impedance	135	150	165	$\Omega$	per Figure 12
Offset			±0.6	Volts	per Figure 10
<b><u>AC Characteristics</u></b>					
Outputs					
Transition Time			40	ns	per Figure 13; 10% to 90%
Propagation Delay					
$t_{PHL}$	40	70	100	ns	per Figures 18 and 19
$t_{PLH}$	40	70	100	ns	per Figures 18 and 19
Max. Transmission Rate	10			Mbps	per Figures 18 and 19
<b>V.35 RECEIVER</b>					
<b><u>DC Characteristics</u></b>					
Inputs					
Input Sensitivity		±80		mV	
Input Impedance	90	100	110	$\Omega$	per Figure 14
Short Circuit Impedance	135	150	165	$\Omega$	per Figure 15
<b><u>AC Characteristics</u></b>					
Inputs					
Propagation Delay					
$t_{PHL}$	50	100	150	ns	per Figures 18 and 21
$t_{PLH}$	50	100	150	ns	per Figures 18 and 21
Max. Transmission Rate	10			Mbps	per Figure 18

# SPECIFICATIONS

Typically 25°C @ V<sub>CC</sub> = +5V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS	
<b>V.11 DRIVER</b>						
<b><u>DC Characteristics</u></b>						
Outputs						
Open Circuit Voltage	±2.0 0.5V <sub>OC</sub>		±6.0	Volts	per Figure 1	
Test Terminated Voltage			±5.0	Volts	per Figure 2	
			0.67V <sub>OC</sub>	Volts		
Balance			±0.4	Volts	per Figure 2	
Offset			±3.0	Volts	per Figure 2	
Short-Circuit Current			±150	mA	per Figure 3	
Power-Off Current			±100	µA	per Figure 5	
<b><u>AC Characteristics</u></b> V <sub>CC</sub> = +5V for AC parameters						
Outputs						
Transition Time			20	ns	per Figure 4; 10% to 90%	
Propagation Delay					Using C <sub>L</sub> =50pF	
t <sub>PHL</sub>	50	80	100	ns	per Figures 18 and 19	
t <sub>PLH</sub>	50	80	100	ns	per Figures 18 and 19	
Differential Skew		20	40	ns	per Figures 18 and 19	
Max. Transmission Rate	10			Mbps		
<b>V.11 RECEIVER</b>						
<b><u>DC Characteristics</u></b>						
Inputs						
Common Mode Range	-7		+7	Volts	per Figures 6 and 7	
Sensitivity			±0.3	Volts		
Input Current			±3.25	mA		
Current w/ 100Ω Term.			±60.75	mA		
<b><u>AC Characteristics</u></b>						
Inputs						
Propagation Delay					Using C <sub>L</sub> =50pF	
t <sub>PHL</sub>	50	110	150	ns	per Figures 18 and 21	
t <sub>PLH</sub>	50	110	150	ns	per Figures 18 and 21	
Differential Skew		20		ns	per Figure 18	
Max. Transmission Rate	10			Mbps		
<b>ENABLE TIMING</b>						
<b><u>Driver</u></b>						
Enable Time						
Enable to Low		90	500	ns	See Figures 16 and 20 C <sub>L</sub> =15pF, S <sub>1</sub> Closed	
Enable to High		90	500	ns		
Disable Time						
Disable From Low		90	500	ns	See Figures 16 and 20 C <sub>L</sub> =15pF, S <sub>1</sub> Closed	
Disable From High		90	500	ns		
<b><u>Receiver</u></b>						
Enable Time						
Enable to Low		90	500	ns	See Figures 17 and 22 C <sub>L</sub> =15pF, S <sub>1</sub> Closed	
Enable to High		90	500	ns		
Disable Time						
Disable From Low		90	500	ns	See Figures 17 and 22 C <sub>L</sub> =15pF, S <sub>1</sub> Closed	
Disable From High		90	500	ns		
<b>POWER REQUIREMENTS</b>						
Supply Voltage V <sub>CC</sub>	+4.75		+5.25	Volts	Driver outputs loaded with 100Ω Driver outputs loaded with 100Ω	
Supply Current I <sub>CC</sub>						
Shutdown				4		µA
V.35 Mode				45		mA
V.11 Mode				95		mA

## TEST CIRCUITS...

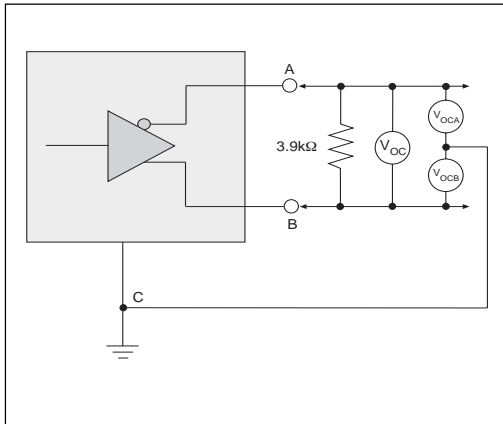


Figure 1. V.11 Driver Output Open-Circuit Voltage

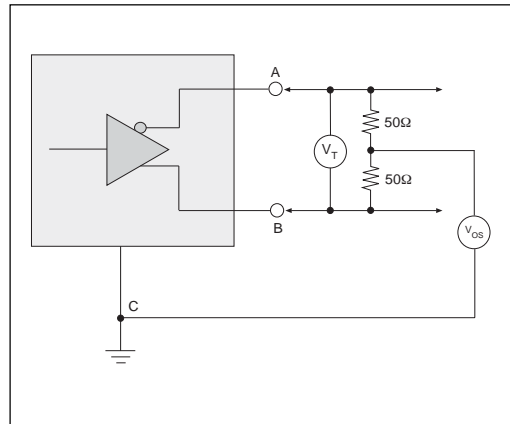


Figure 2. V.11 Driver Output Test Terminated Voltage

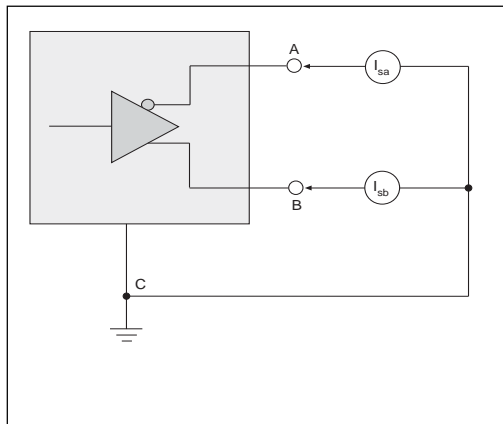


Figure 3. V.11 Driver Output Short-Circuit Current

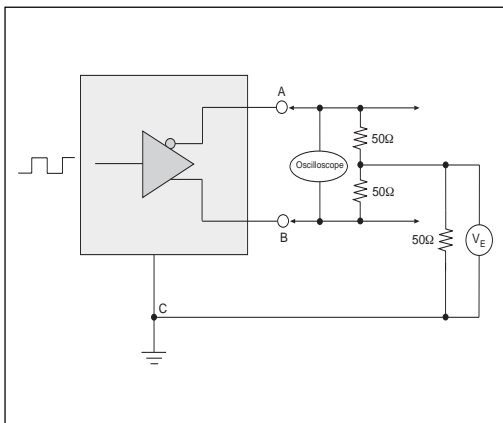


Figure 4. V.11 Driver Output Rise/Fall Time

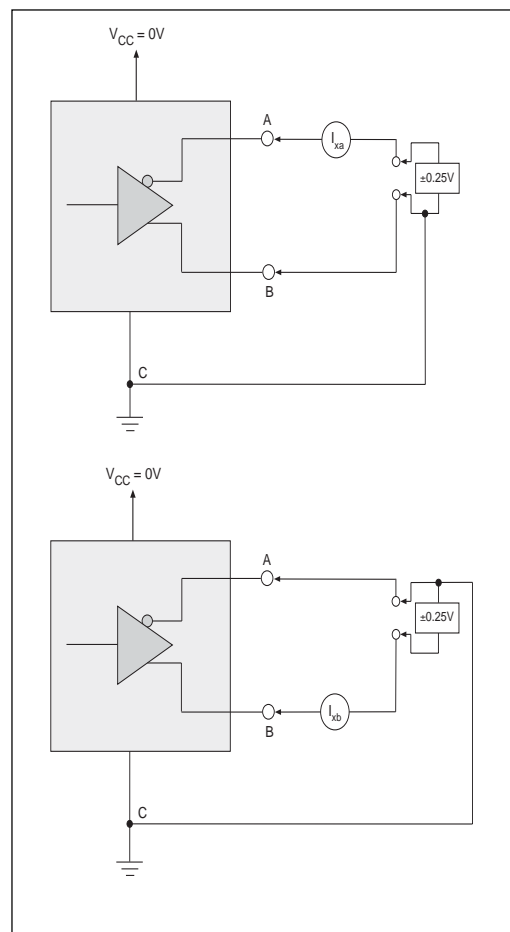


Figure 5. V.11 Driver Output Power-Off Current

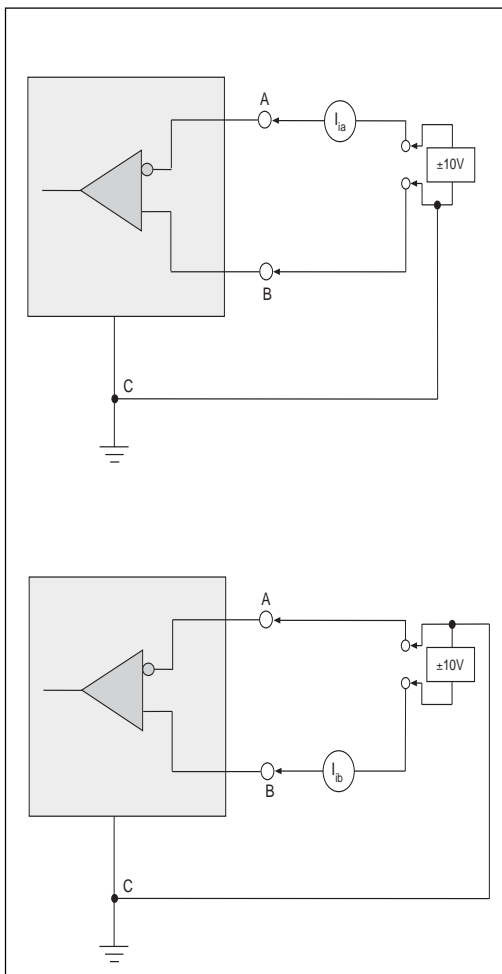


Figure 6. V.11 Receiver Input Current

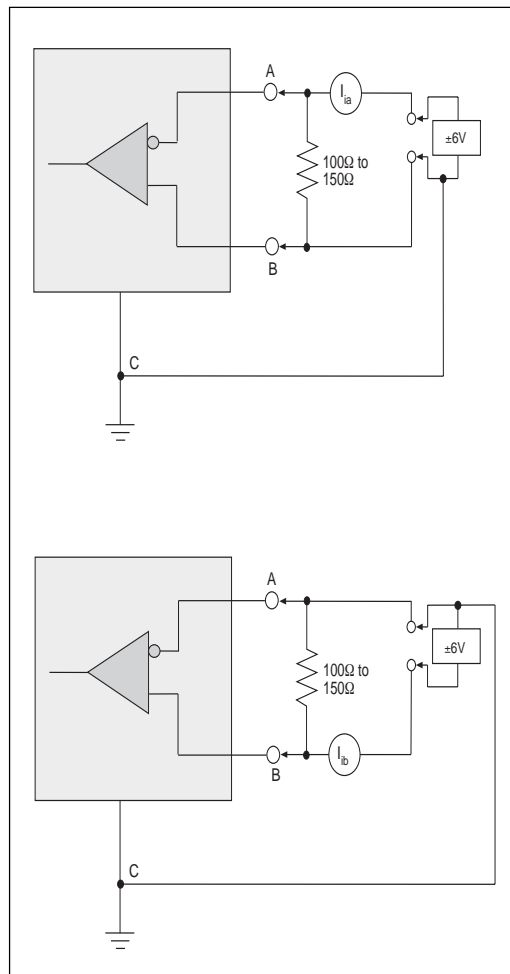


Figure 8. V.11 Receiver Input Current w/ Termination

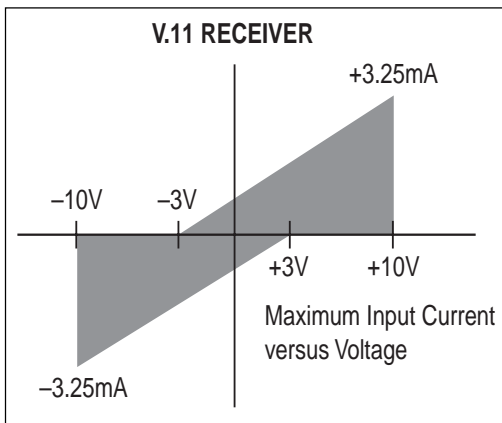


Figure 7. V.11 Receiver Input IV Graph

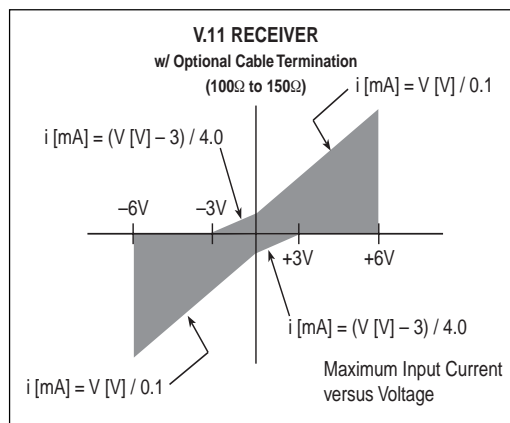
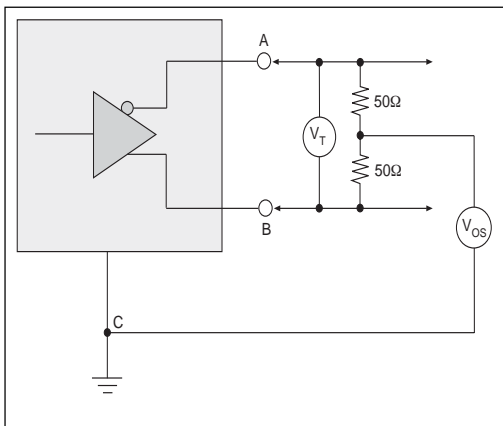
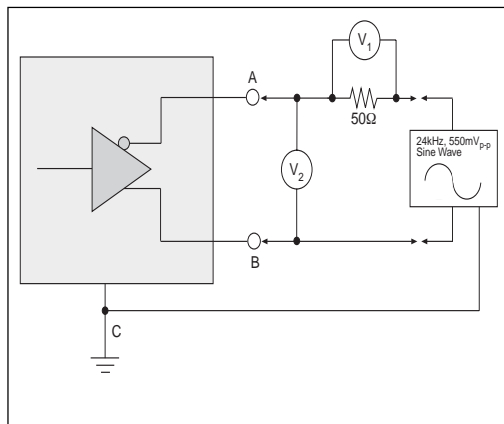


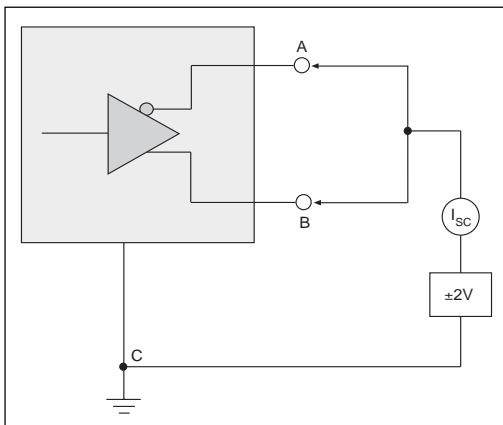
Figure 9. V.11 Receiver Input Graph w/ Termination



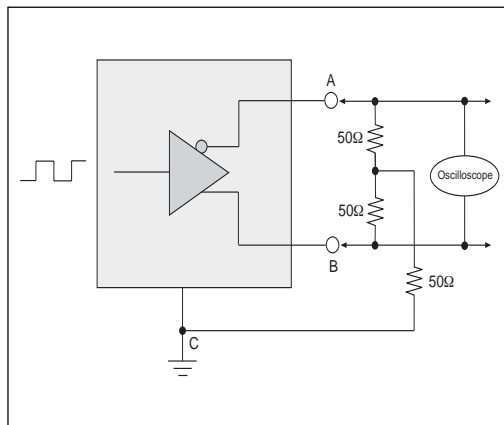
**Figure 10. V.35 Driver Output Test Terminated Voltage**



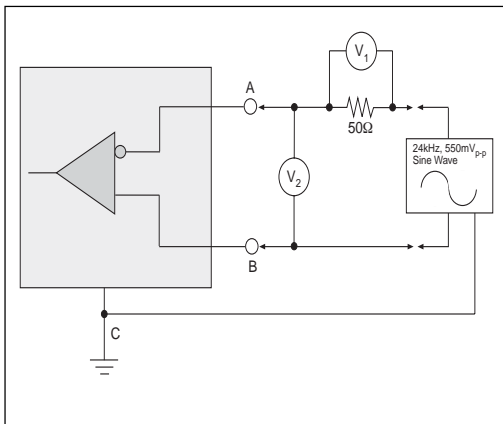
**Figure 11. V.35 Driver Output Source Impedance**



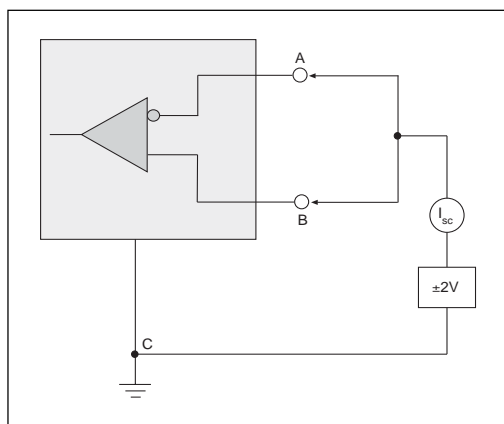
**Figure 12. V.35 Driver Output Short-Circuit Impedance**



**Figure 13. V.35 Driver Output Rise/Fall Time**



**Figure 14. V.35 Receiver Input Source Impedance**



**Figure 15. V.35 Receiver Input Short-Circuit Impedance**

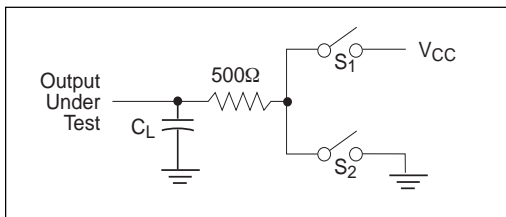


Figure 16. Driver Timing Test Load #2 Circuit

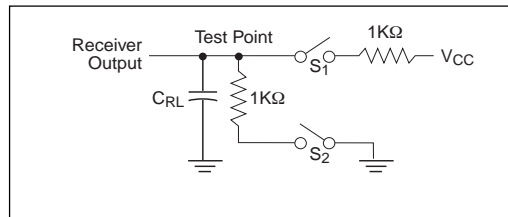


Figure 17. Receiver Timing Test Load Circuit

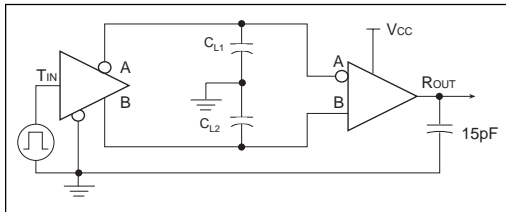


Figure 18. Driver/Receiver Timing Test Circuit

## SWITCHING WAVEFORMS...

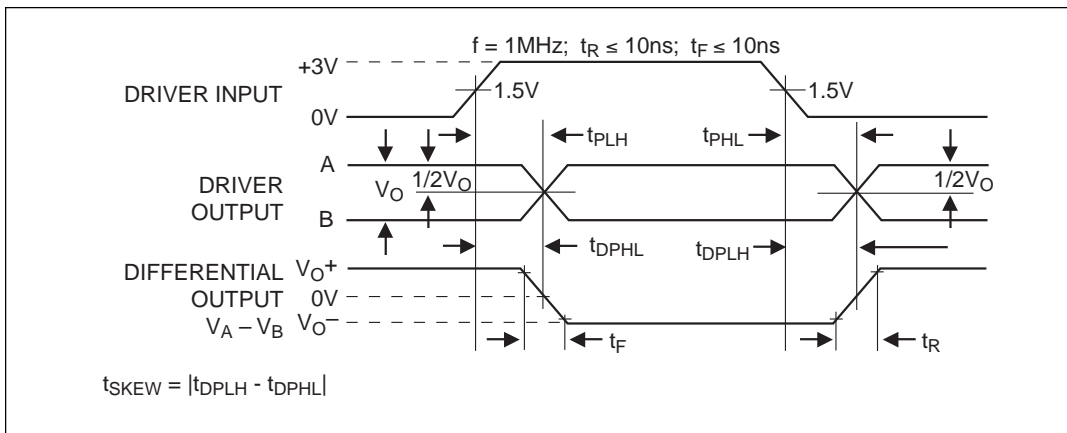


Figure 19. Driver Propagation Delays

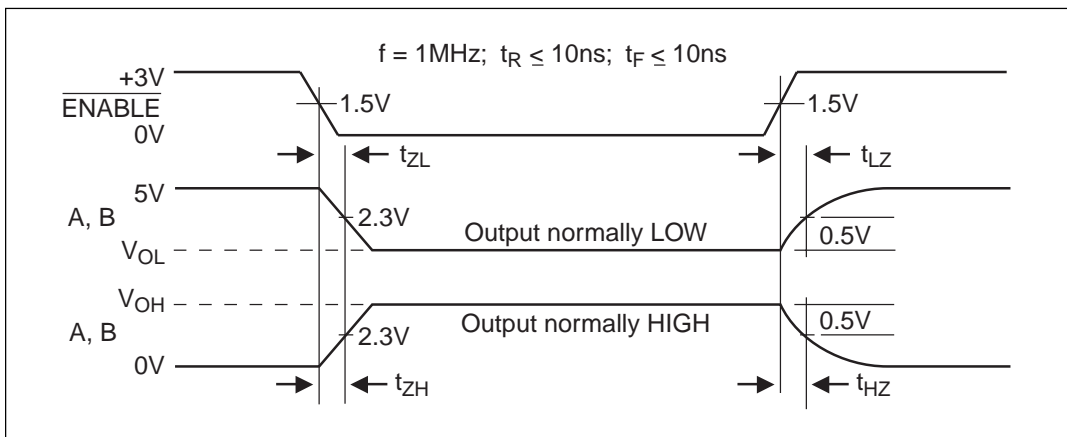


Figure 20. Driver Enable and Disable Times

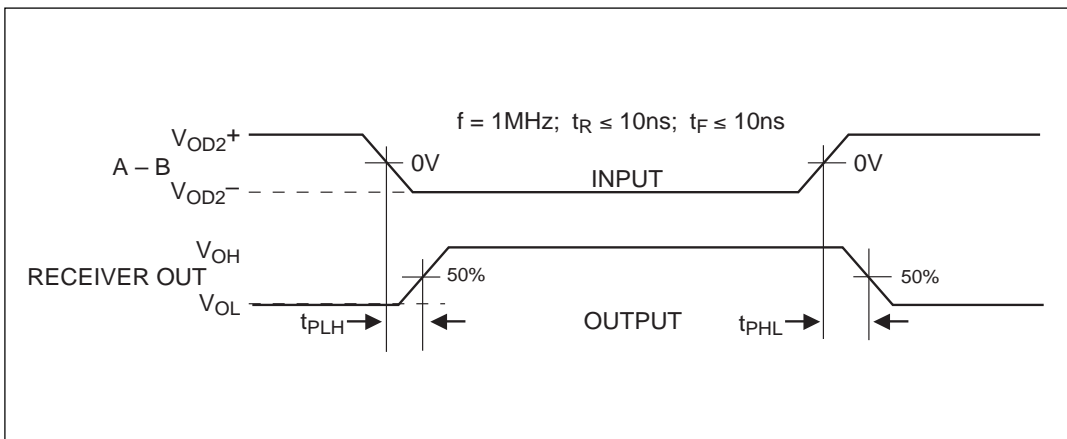


Figure 21. Receiver Propagation Delays

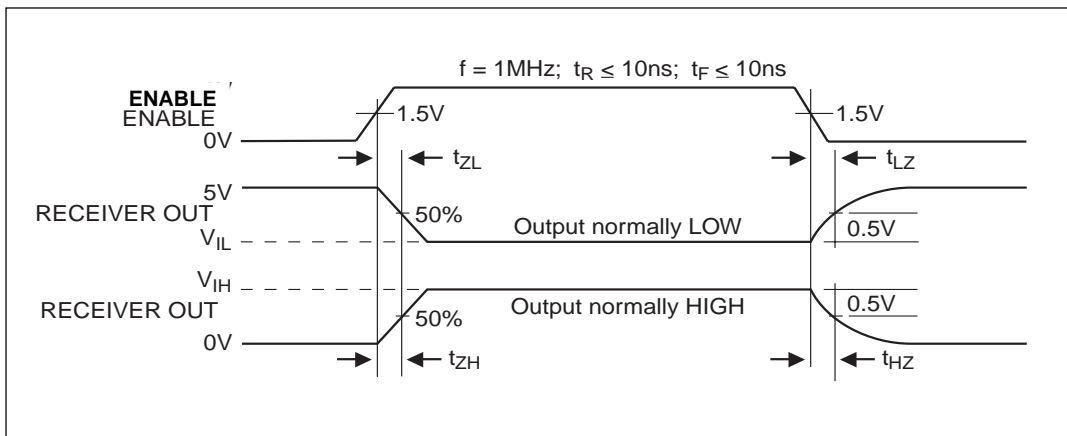


Figure 22. Receiver Enable and Disable Times

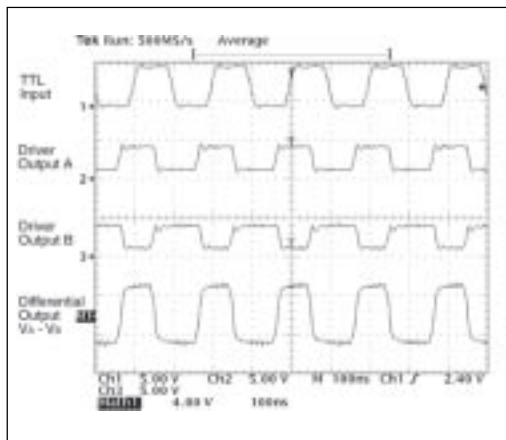


Figure 23. Typical V.11 Driver Output

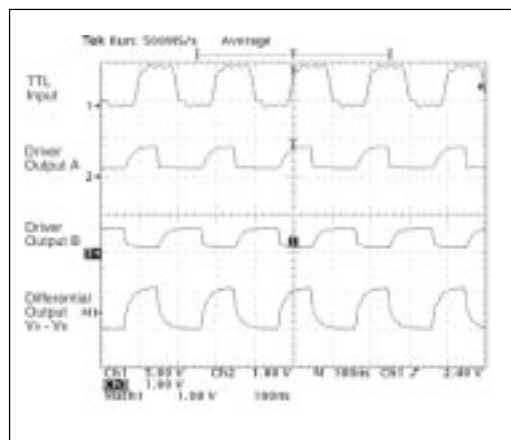
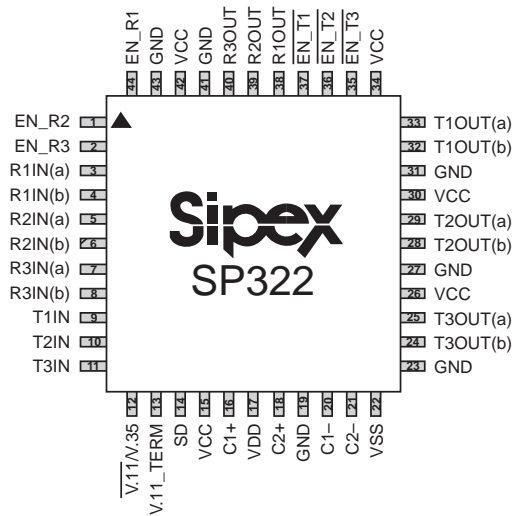
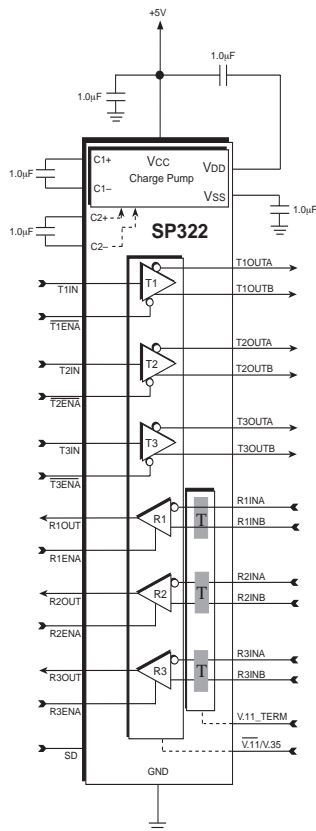


Figure 24. Typical V.35 Driver Output





**Figure 25. SP322 Pinout**



**Figure 26. SP322 Typical Operating Circuit**

## THEORY OF OPERATION

The **SP322** is a programmable V.11 or V.35 transceiver IC. It contains three driver and three receivers which can be configured to either V.11 or V.35 physical layer electrical characteristics. The transceivers within the **SP322** include all the necessary termination resistor networks required for compliant V.11 and V.35 signals. This simplifies serial port designs using V.11 or V.35 where the engineer does not have to configure V.11 cable termination resistors and the V.35 network.

The **SP322** contains four basic blocks: the charge pump, differential drivers, differential receivers, termination network circuitry. Each block is described in the following.

### Charge-Pump

The **SP322** charge pump is smaller version of the **Sipex**—patented design (U.S. 5,306,954). The charge pump still requires four external capacitors and uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. But the pump is only used for providing internal biasing for the transceivers and the termination circuitry. The  $V_{DD}$  and  $V_{SS}$  outputs provide only 3mA of output current and should not be connected to bias other external circuitry.

Recommended charge pump capacitor values are 1 $\mu$ F or greater. The internal oscillator provides a clock rate for the charge pump which typically operates at 15kHz.

### Drivers

The **SP322** has three differential drivers. There are two types of drivers includes within the **SP322**: V.11 drivers and V.35 drivers.

When configured in V.11 mode, the V.11 drivers produce a differential output compliant with the V.11 and RS-422 electrical specifications. This includes the all the DC electrical parameters such as  $V_{OC}$ ,  $V_T$ ,  $V_{OS}$ , etc. The strength of the SP322 drivers allow them to also drive signals per the RS-485 standard. The  $V_T$  minimum of  $\pm 1.5V$  is provided by the driver output given a load of 54 $\Omega$  as opposed to  $\pm 2.0V$  with a 100 $\Omega$  load for RS-422. However, the drivers are not intended to operate over the RS-485 common mode range of +12V to -7V. The common

mode range for the V.11 drivers is +7V to -7V which is in accordance to the ITU V.11 specification.

When in V.35 mode, the drivers provide V.35 signals compliant to the ITU V.35 electrical specification. Specifically, the V.35 driver is designed to supply a differential output of  $\pm 0.55V$  with an offset of less than 0.6V. With **Sipex's** patent-pending V.35 driver design, the driver also adheres to impedance measurements such as driver output source impedance (100 $\Omega \pm 50\Omega$ ) and driver output short-circuit impedance (150 $\Omega \pm 15\Omega$ ). Traditional V.35 drivers require a resistor network to provide the proper V.35 impedance specifications for the driver outputs. The **SP322** V.35 driver does this without the aid of any external components attached to the driver output. Its unique design contains internal resistance matching and switching to provide compliant V.35 signals.

Each driver includes an enable pin for added convenience. The driver enable pins are low active and will tri-state the driver outputs if a logic "1" is applied. During this state, the drivers are high impedance. The enable pins include a pull-down resistor so that the pin can be unconnected where the driver will always be enabled. Regardless of physical protocol, the drivers can operate to at least 10Mbps.

### Receivers

The **SP322** has three differential receivers which are used for either V.11 or V.35. The receivers have a 200mV sensitivity and operate over the common mode range of +7V to -7V. The receiver itself is the same in either V.11 or V.35 mode. The receiver input termination is configured differently for each mode (V.11/V.35 pin).

The receivers also include enable pins for convenience. The receiver enable pins are high active where a logic "0" will tri-state the receiver outputs. During tri-state, the receiver inputs are approximately 12k $\Omega$ . Any termination associated with the operating mode is disconnected during tri-state of that receiver. The receiver enable pins have a pull-up resistor that allows the pins to be unconnected. The receiver will always be active in this case. The differential receiver can operate to at least 10Mbps.

## Termination Circuitry

Unique to **Sipex**, the **SP322** provides internal resistor networks for V.35 as well as the cable termination for V.11. The resistor network for the V.35 receivers are configured as a typical V.35 receiver using two  $51\Omega$  resistors in series tied to the A and B inputs with a  $124\Omega$  center-tap resistor to ground. The network is internally switched on during V.35 mode ( $\overline{V.11/V.35} = V_{CC}$ ) using high performance, low  $r_{ON}$  transistors. The transistors can operate efficiently over +7V to -7V, and can tolerate over +10V to -10V without damage. This termination provides the proper V.35 receiver input impedance of  $100\Omega$  and short-circuit impedance at 2V of  $150\Omega$  with 10% accuracy.

The configuration for the V.11 receiver input resistor network is similar to the V.35 network except that the  $124\Omega$  resistor is disconnected ( $\overline{V.11/V.35} = 0V$ ). A series resistor is also added increase the input impedance to over  $120\Omega$  for the V.11 cable termination. The minimum resistance per the ITU V.11 specification is  $100\Omega$ . The V.11 termination can be switched off using the V.11\_TERM pin. For a terminated V.11 receiver, this pin is at a logic "1". A logic "0" will inform the switches to disconnect the V.11 termination.

## Shutdown

The **SP322** includes a shutdown pin (SD) which disables the charge pump and all power consuming circuitry to provide low  $I_{CC}$ . A logic "1" to the SD pin will shut down the **SP322** where it will draw less than  $20\mu A$  of current.

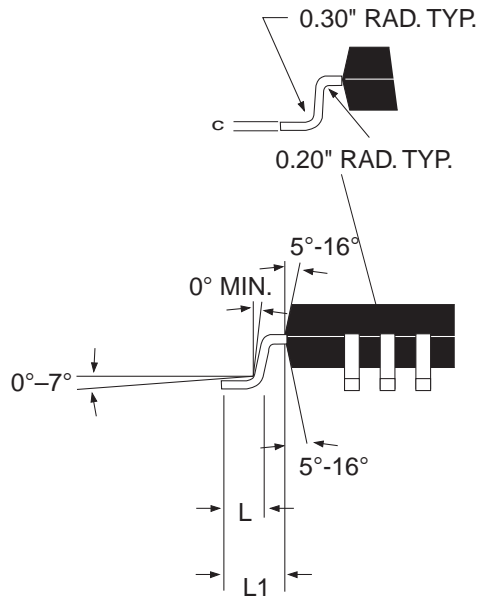
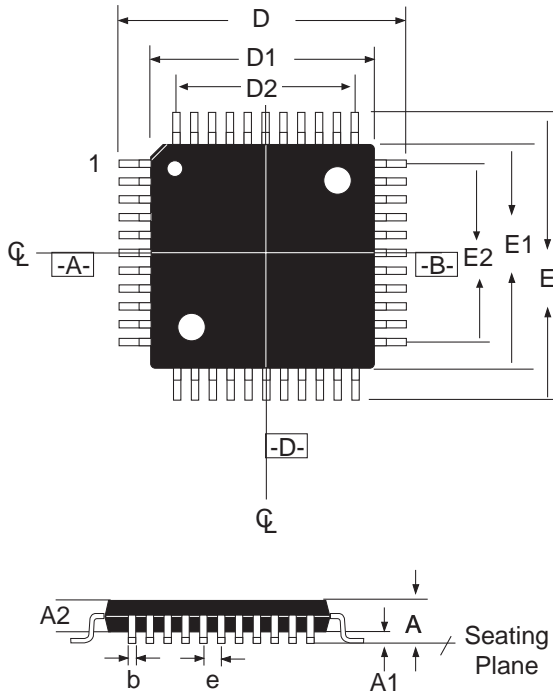
## NET1/2 European Compliance

As with all of **Sipex's** previous multi-protocol transceiver ICs, the **SP322** drivers and receivers have been designed to meet all electrical specifications for ITU V.11 and V.35. Furthermore, it is internally tested and will pass the NET1/2 physical layer testing requirements. Please note that although the **SP322** adheres to NET1/2 testing, any complex or unusual configuration should be double-checked to ensure NET compliance. Consult factory for details.

## Applications Information

The **SP322** is designed for serial port applications needing V.11 and V.35 transceivers. The **SP322** supports a variety of physical layer protocols such as EIA-530, EIA-530A, RS-449, and V.36 where V.11 transceivers are used for clock and data signals. The termination resistors are recommended for crosstalk and reflections elimination under higher speed operation. Internal termination solves many headaches and configuration hassles with implementing V.11 and V.35. The **SP322** provides a simple, low-cost solution for the clock and data lines for synchronous serial ports. The handshaking lines such as CTS, DTR, etc. can be implemented using discrete RS-422 or RS-232 transceivers, depending on the mode supported. **Sipex** supplies either differential (V.11) or single-ended (V.28) discrete transceiver products to mate with the **SP322**.

# PACKAGE: 44 Pin MQFP

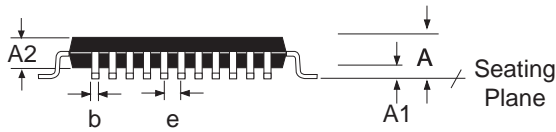
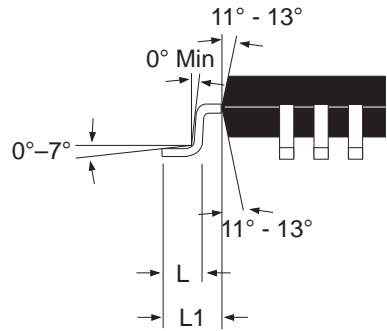
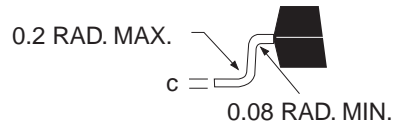
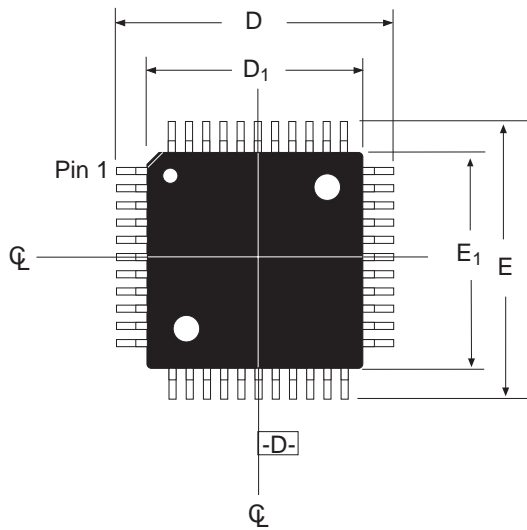


DIMENSIONS Minimum/Maximum (mm)	44-PIN MQFP JEDEC MS-022 (AB) Variation		
SYMBOL	MIN	NOM	MAX
A			2.45
A1	0.00		0.25
A2	1.80	2.00	2.20
b	0.29		0.45
D	13.20 BSC		
D1	10.00 BSC		
D2	8.00 REF		
E	13.20 BSC		
E1	10.00 BSC		
E2	8.00 REF		
e	0.80 BSC		
N	44		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.73	0.88	1.03
L1	1.60 BASIC		

## 44 PIN MQFP (MS-022 BC)

# PACKAGE: 44 Pin LQFP



DIMENSIONS Minimum/Maximum (mm)	44-PIN LQFP JEDEC MS-026 (BCB) Variation		
SYMBOL	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.50
D	12.00 BSC		
D1	10.00 BSC		
e	0.80 BSC		
E	12.00 BSC		
E1	10.00 BSC		
N	44		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.45	0.60	0.75
L1	1.00 BASIC		

44 PIN LQFP

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP322CF .....	0°C to +70°C .....	44-pin MQFP

Please consult the factory for pricing and availability on a Tape-On-Reel option.



### ANALOG EXCELLENCE

#### Sipex Corporation

##### Headquarters and Sales Office

233 South Hillview Drive  
Milpitas, CA 95035  
TEL: (408) 934-7500  
FAX: (408) 935-7600

##### Sales Office

22 Linnell Circle  
Billerica, MA 01821  
TEL: (978) 667-8700  
FAX: (978) 670-9001  
e-mail: sales@sipex.com

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